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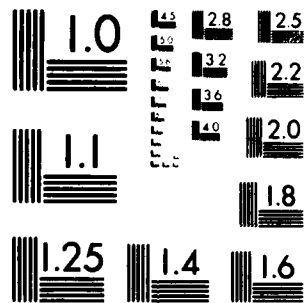
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WIDEBAND HF CHANNEL ANALYZER

Final Report

January 1981

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Prepared for

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<p>This document is a final report describing a wideband (1 MHz) HF channel analyzer. The Wideband HF Channel Analyzer is a digital signal processor designed to be used for wideband high-frequency radio channel measurement studies. The analyzer contains analog-to-digital converters, a digital pre-processor, a digital correlator array, a digital post-processor and two</p>		

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computer interfaces.

/ To perform a channel measurement experiment, a transmitter at a remote site broadcasts a pseudo-random number (PN) sequence modulated onto a suitable carrier. After complex demodulation at the receiver, the analyzer measures channel delay by correlating the received sequence with its internal reference. Two modes of operation are provided. The Sounder Mode is used to obtain a preliminary characterization of the channel. The Prober Mode is used to more accurately measure the channel delay characteristics.

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## SECTION 1

### INTRODUCTION

The Wideband HF Channel Analyzer is a digital signal processor designed to be used for wideband high-frequency radio channel measurement studies. The analyzer contains analog-to-digital converters, a digital pre-processor, a digital correlator array, a digital post-processor and two computer interfaces.

To perform a channel measurement experiment, a transmitter at a remote site broadcasts a pseudo-random number (PN) sequence modulated onto a suitable carrier. After complex demodulation at the receiver, the analyzer measures channel delay by correlating the received sequence with its internal reference. Two modes of operation are provided. The Sounder Mode is used to obtain a preliminary characterization of the channel. The Prober Mode is used to more accurately measure the channel delay characteristics.

The Wideband HF Channel Analyzer is shown in Figures 1.1, 1.2, and 1.3. It is a self-contained unit and is designed to operate between an HF receiver with in-phase and quadrature (I and Q) outputs and a computer for data display and recording.

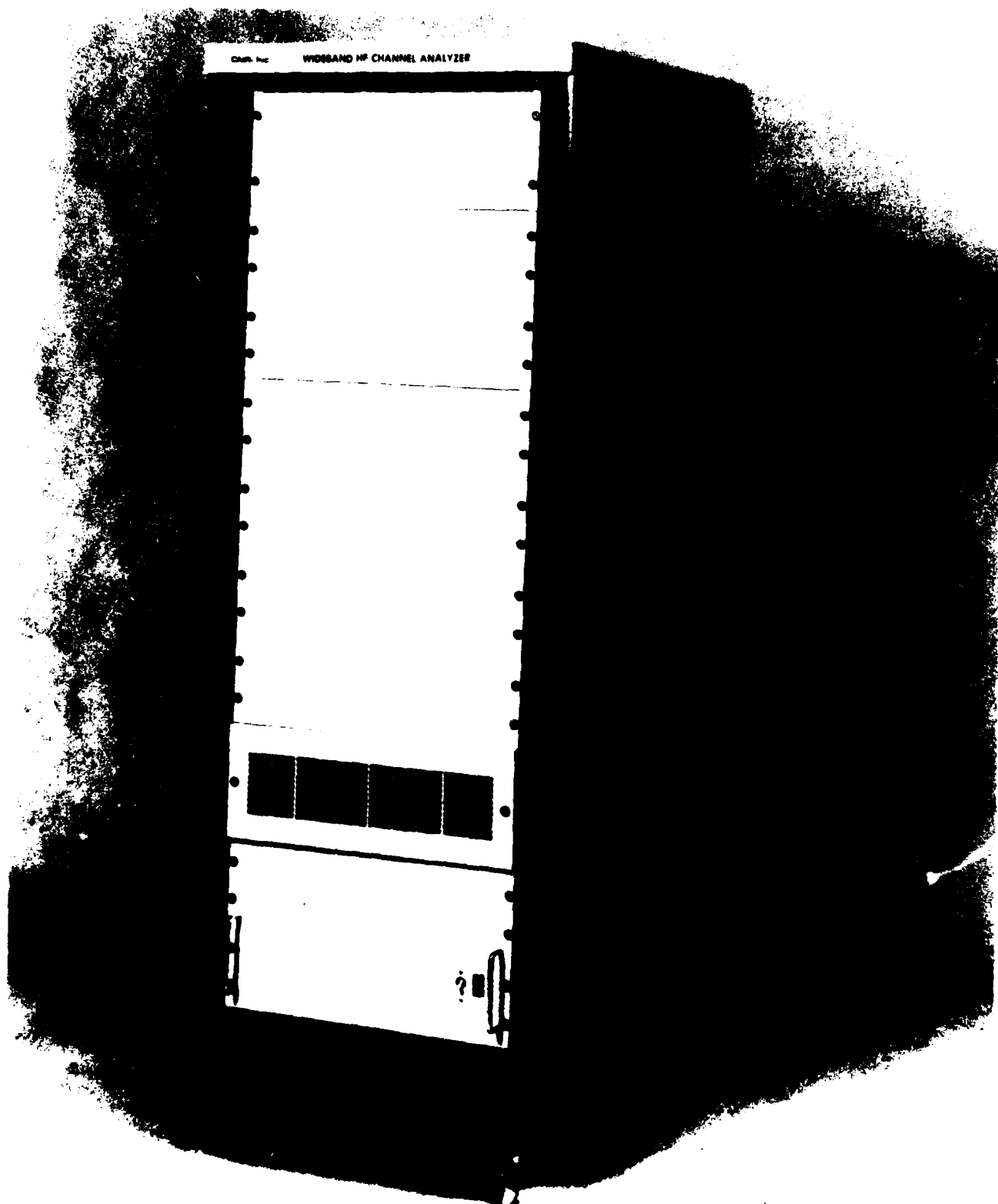


Figure 1.1 Wideband HF Channel Analyzer

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WIDEBAND HF CHANNEL ANALYZER

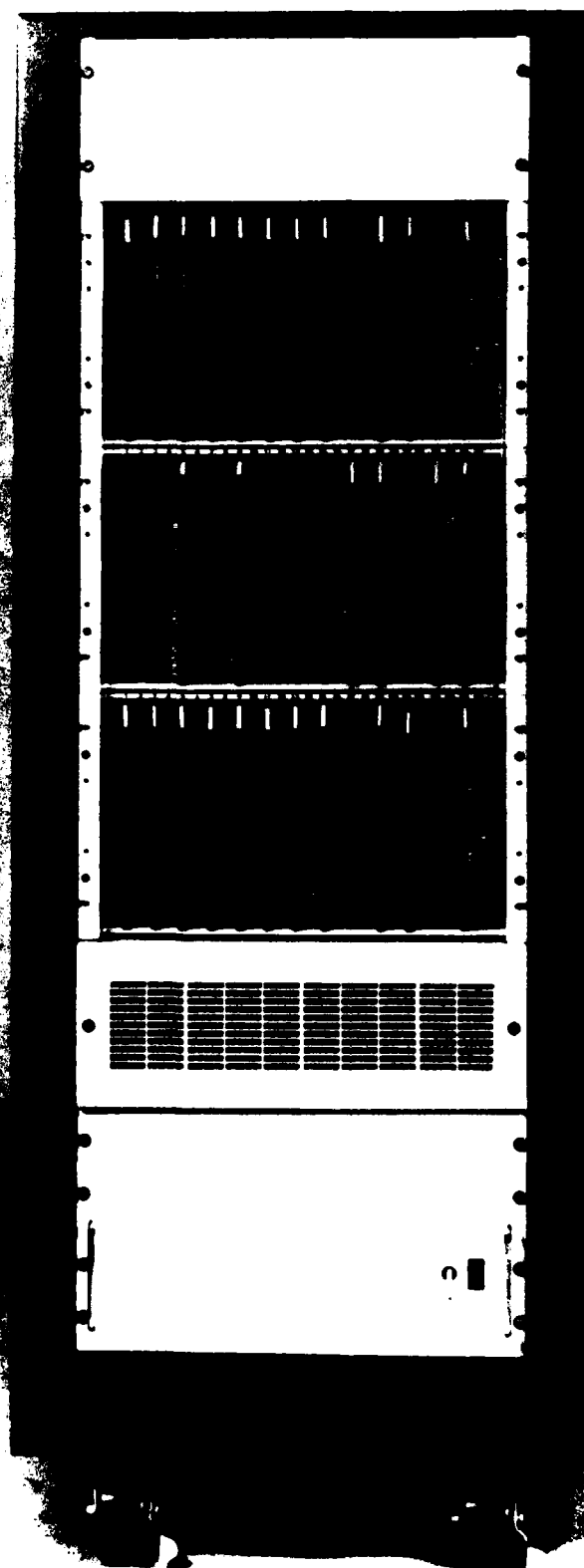


Figure 1.2 Wideband HF Channel Analyzer with Front Panels Removed



Figure 1.3 Wideband HF Channel Analyzer with Side  
Panel and Rear Door Removed

## SECTION 2

### INSTALLATION

Connections to the Wideband HF Channel Analyzer are made via the rear panel. Figure 2.1 shows the rear panel of the analyzer. Interface specifications are listed below.

#### AC Power:

125 VAC, 60 Hz, 30 amp, single-phase circuit.  
Power cord with three-prong twist-lock connector provided.

#### Clock:

8 MHz TTL compatible square wave. BNC connector on rear panel. 50 ohm termination provided (removable).

#### Analog Inputs:

I and Q inputs via BNC connectors.  $\pm 5$  volts maximum. Overvoltage:  $\pm 15$  volts maximum.  
Provision for optional terminating resistors on A/D converter cards.

#### Computer Interface:

Interface is to a DEC PDP-11 computer with two DR11-C general device interface cards. Connection is through four DEC compatible H854 40 pin male connectors as follows:

J1 to J1 of DR11-C (Control and Data Interface)  
J2 to J2 of DR11-C (Control and Data Interface)

J3 to J1 of DR11-C (AGC Interface)

J4 to J2 of DR11-C (AGC Interface)

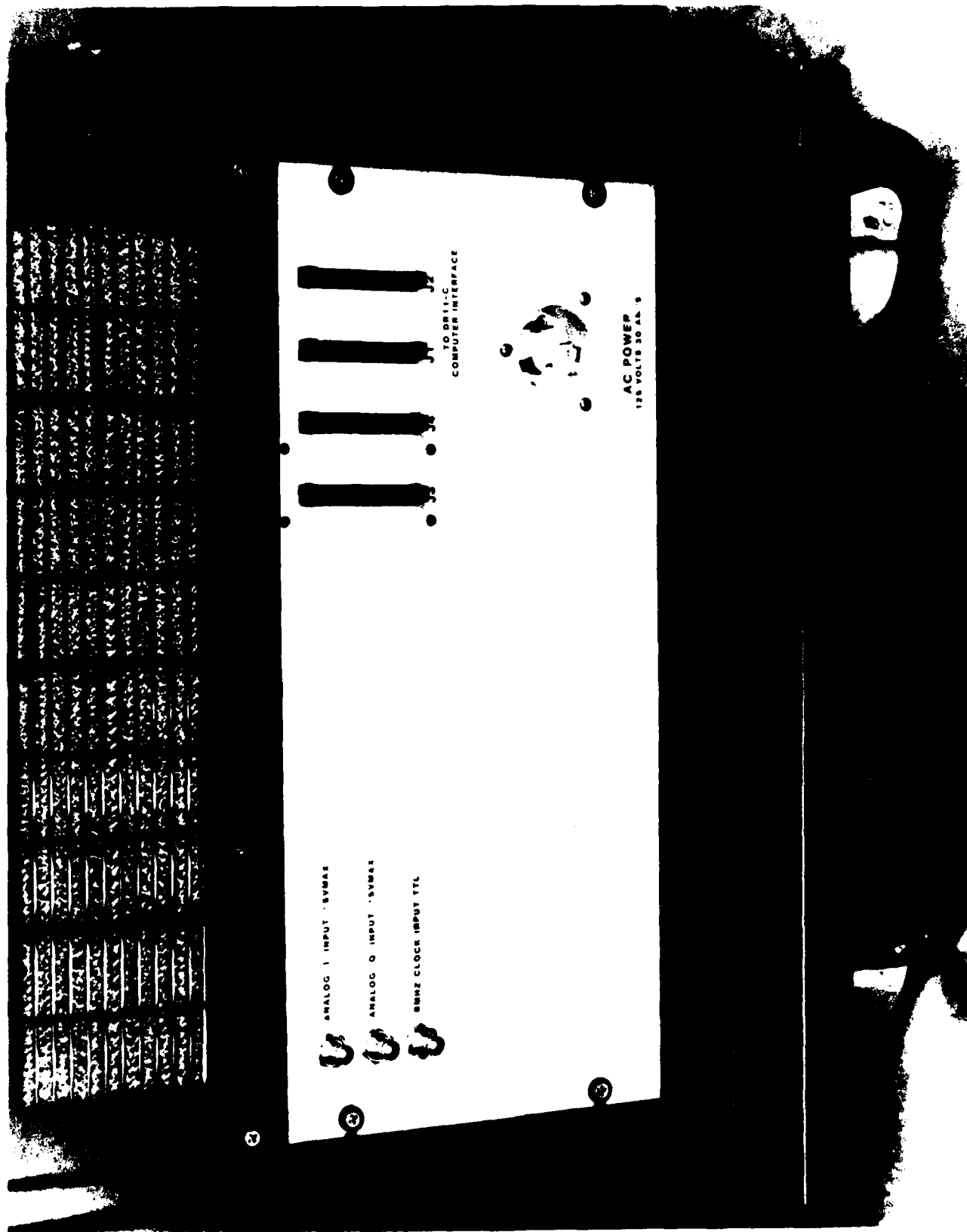


Figure 2.1 Wideband HF Channel Analyzer Rear Panel

## SECTION 3

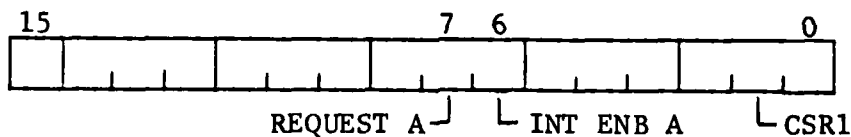
### OPERATION

Except for the power switch, the Wideband HF Channel Analyzer is controlled entirely by the computer through two DR11-C interface cards. One DR11-C is connected to J1 and J2 on the rear panel of the analyzer. This is the control and data interface. The other DR11-C is connected to J3 and J4. This is the AGC data interface. The following paragraphs define these interfaces and describe their use in controlling the analyzer. Following this description is a flowchart of typical operation, Figure 3.1.

#### 3.1 Control and Data Interface

The control and data interface is the primary interface between the Wideband HF Channel Analyzer and the computer. The three registers of the DR11-C connected to J1 and J2 on the analyzer are used to send control data to the analyzer and to receive delay tap gain data from the analyzer. In addition to the register data, the DR11-C generates several control signals which are used by the analyzer. The following is a description of the use of these registers and control lines.

##### 3.1.1 DRCSR (Control and Status Register)



CSR1 is controlled by the computer and read by the analyzer.

CSR1 = 0 puts the analyzer into the IDLE state.



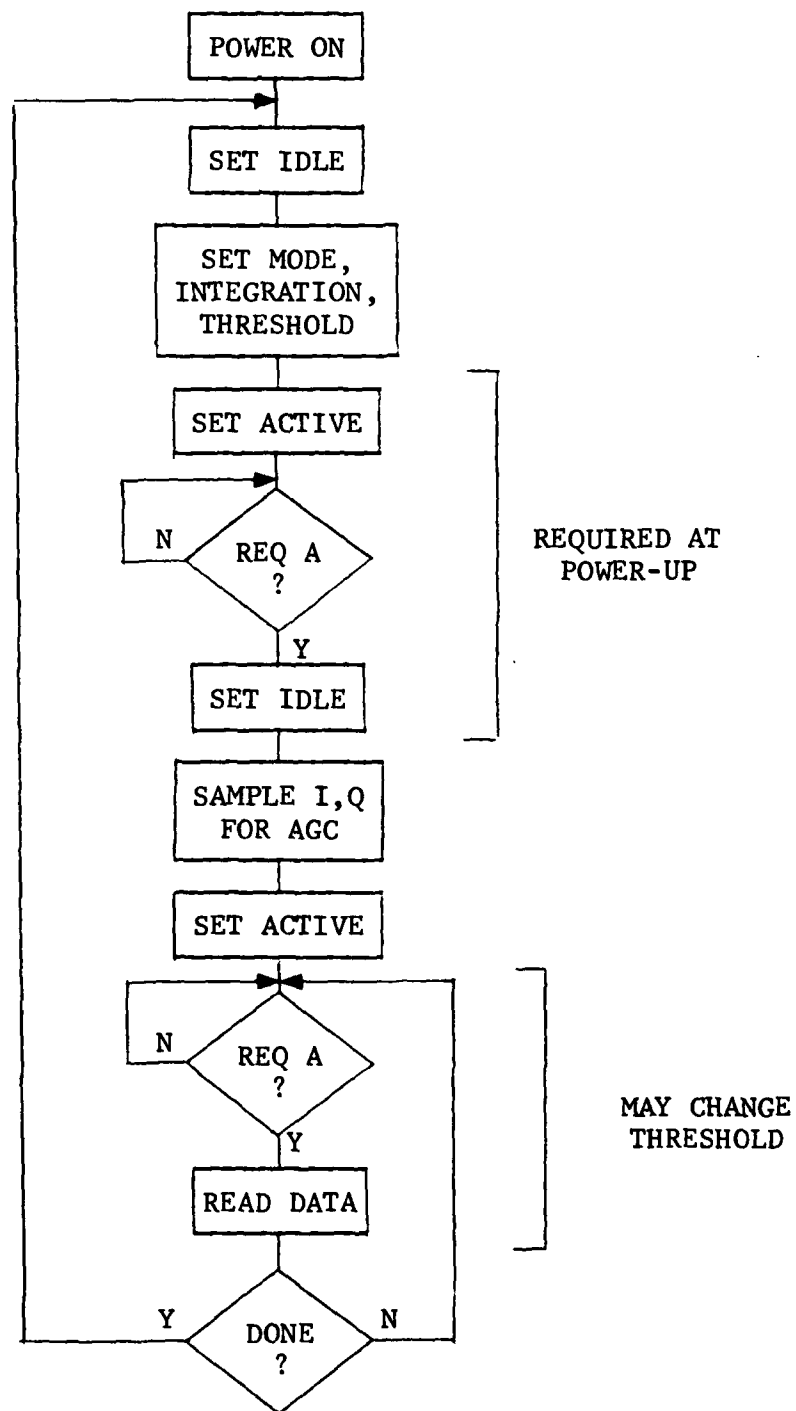


Figure 3.1 Flowchart of Typical Operation, Wideband HF Channel Analyzer

CSR1 = 1 puts the analyzer into the ACTIVE state.

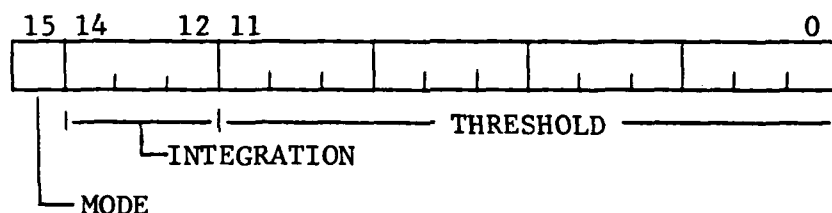
INT ENB A is controlled by the computer but is not read by the analyzer.

INT ENB A = 1 causes the DR11-C to generate an interrupt when it receives REQUEST A = 1. This is the normal mode of operating the analyzer.

REQUEST A is controlled by the analyzer.

REQUEST A = 1 is sent when there is data present at the output of the analyzer.

### 3.1.2 DROUTBUF (Transmit Output Buffer)



DROUTBUF is used by the computer to transmit control parameters to the analyzer. When DROUTBUF is loaded by the computer, the DR11-C generates a pulse signal, NEW DATA READY. NEW DATA READY is used by the analyzer to strobe in the parameters. There are restrictions on changing parameters which are described below.

MODE = 1 selects SOUNDER MODE.

MODE = 0 selects PROBER MODE.

MODE can only be changed when the analyzer is in the IDLE state (CSR1 = 0). The MODE bit is not strobed in by NEW DATA READY unless the analyzer is in the IDLE state.

INTEGRATION is a 3-bit code used to specify the number of sequences to be integrated at the input of the analyzer prior to correlation. The code is (in octal):

- 7 - single sequence
- 6 - two sequences
- 4 - four sequences
- 0 - eight sequences

INTEGRATION can only be changed when the analyzer is in the IDLE state.

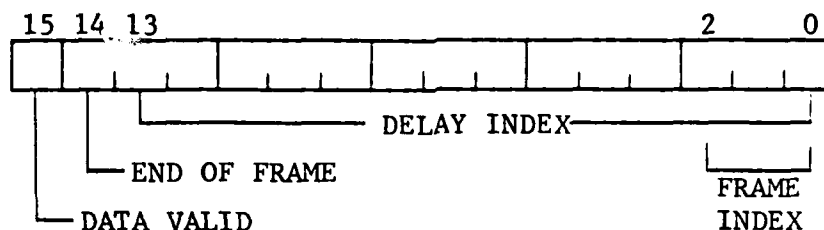
THRESHOLD is an unsigned 12-bit integer. The magnitude of the 12 most significant bits (excluding the sign bit) of the I and Q correlator outputs are compared to the THRESHOLD. If either the I value or the Q value is strictly greater than the THRESHOLD, both values are sent to the computer.

### 3.1.3 DRINBUF (Receiver Input Buffer)

DRINBUF is used by the computer to receive data from the analyzer. The analyzer asserts REQUEST A to signal the computer that there is data present at the interface. Three words are sent for each delay: the Tap Gain Index, the I voltage, and the Q voltage. All transfers are in multiples of three words. When the computer responds to REQUEST A, the DR11-C generates a pulse signal DATA TRANS. DATA TRANS is used by the analyzer to advance the next word to the interface. If, after the third word is sent, there is more data to be transferred, the analyzer continues to assert REQUEST A. Otherwise, REQUEST A is dropped when the third word has been transferred.

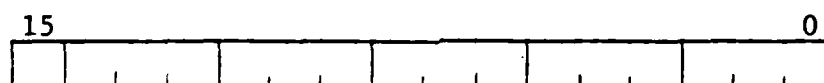
The three words sent to the computer for each delay tap gain are:

### Tap Gain Index



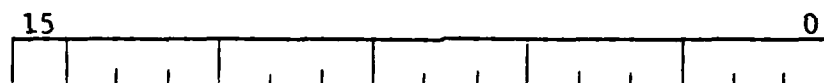
These fields are described below.

### I Voltage



16 bit 2's complement integer

### Q Voltage



16 bit 2's complement integer

### Data Valid Bit:

The Data Valid Bit is set each time valid data is strobed into the FIFO memory. Data is considered valid if either the I or Q value exceeds threshold or if the Tap Gain Index is an End of Frame marker.

### End of Frame:

An End of Frame marker is generated when all correlations for a given Frame have been computed and compared to the threshold (2,047 correlations in the Prober Mode; 255 correlations in the Sounder Mode). The I and Q values sent to

the computer with the End of Frame marker are redundant values that are not compared to the threshold.

A Scan consists of eight Frames. The End of Frame marker for Frame 7 also signals the end of the Scan.

Delay Index:

Each tap gain value is tagged with a Delay Index. The identification of tap 0 by the Wideband HF Channel Analyzer hardware is not related to the radio propagation path, but is held fixed with respect to an internal reference.

A Prober Mode Scan of eight frames of 2,047 correlations produces estimates for 16,376 taps spaces at 0.5  $\mu$ sec intervals around an 8.188 ms delay ambiguity circle. Each unit of the Delay Index represents 0.5  $\mu$ sec of delay.

The 14-bit index represents more than one turn around the delay ambiguity circle. The taps at  $37770_8 - 37777_8$  are redundant with those at  $00000_8 - 00007_8$ . The redundant tap gain values are actually computed. The tap gain values at  $37770_8 - 37777_8$  are compared to the threshold and if either the I or Q value exceeds the threshold are sent to the computer as data. The I and Q values at  $00000_8 - 00000_7$  are sent to the computer with the End of Frame marker.

The taps for the Prober Mode are computed in the following order:

$37770_8 - 00000_8$   
 $37771_8 - 00001_8$   
 $37772_8 - 00002_8$   
 $37773_8 - 00003_8$   
 $37774_8 - 00004_8$

37775<sub>8</sub> - 00005<sub>8</sub>

37776<sub>8</sub> - 00006<sub>8</sub>

37777<sub>8</sub> - 00007<sub>8</sub>

The least significant octal digit is the Frame Index.

The Sounder Mode Scan of eight frames of 255 correlations produces estimates for 2,040 taps spaced at 4.0  $\mu$ sec around an 8.160 ms delay ambiguity circle. Each unit of the Delay Index represents 4.0  $\mu$ sec. As in the Prober Mode, redundant taps are computed. The taps for the Sounder Mode are computed in the following order:

03770<sub>8</sub> - 00000<sub>8</sub>

03771<sub>8</sub> - 00001<sub>8</sub>

03772<sub>8</sub> - 00002<sub>8</sub>

03773<sub>8</sub> - 00003<sub>8</sub>

03774<sub>8</sub> - 00004<sub>8</sub>

03775<sub>8</sub> - 00005<sub>8</sub>

03776<sub>8</sub> - 00006<sub>8</sub>

03777<sub>8</sub> - 00007<sub>8</sub>

The least significant octal digit is the Frame Index.

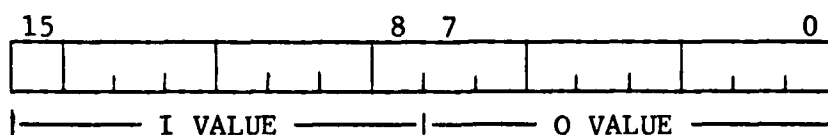
### 3.2 AGC Computer Interface

The AGC Computer Interface allows the computer to asynchronously sample the I and Q analog inputs to the analyzer during the IDLE state. This interface operates through a second DR11-C connected to J3 and J4 on the rear panel of the analyzer. This DR11-C must be assigned a different address than the Control and Data Interface.

The I and Q analog inputs are sampled by reading the DRINBUF of the DR11-C. This generates a DATA TRANS pulse which is used to strobe the I and Q channel analog-to-digital converters. DATA TRANS is ignored unless the analyzer is in the IDLE state. The first read is performed only to generate DATA TRANS. The data read is not valid.

When DATA TRANS is received, the A/D converters are commanded to sample and convert. When the conversion is complete, the data is held and REQUEST A is asserted. When this data is read, as signaled by DATA TRANS, REQUEST A is dropped and a new conversion is initiated. Since the A/D converters are much faster than the computer, data may be taken at a rate limited by the computer and the DR11-C.

The I and Q sample values are packed into a single 16-bit word for transfer to DRINBUF. The I and Q values are each 8 bit 2's complement numbers. Full scale represents approximately 5 volts.



## SECTION 4

### SYSTEM LEVEL DESCRIPTION

The Wideband HF Channel Analyzer is a high-speed digital integrator and correlator designed to compute delay tap gain characteristics of a wideband high-frequency radio channel. The input to the digital processor is from an analog high-frequency radio receiver. The in-phase and quadrature components of the received waveform are converted to digital values and correlated with all positions of a reference pseudo-random number sequence identical to the one transmitted. Correlated values below an adjustable threshold are rejected. Those tap gain values above the threshold are transferred to a mini-computer for further analysis, display, and recording.

Two modes of operation are provided. The Sounder Mode is used to obtain a preliminary characterization of the channel. The Prober Mode is used to more accurately measure the channel delay characteristics.

Corresponding samples from two, four, or eight received sequences can be integrated before being correlated with the reference sequence. Integration improves the signal-to-noise ratio of the received waveform but slows the computation of tap gains.

The Wideband HF Channel Analyzer is a self-contained unit with its own cabinet and power supplies. In addition to the



analog input from the receiver, the analyzer receives a coherent clock. The minicomputer sets the mode and integration and specifies a threshold for tap gain selection.

This section describes the system aspects of the Wideband HF Channel Analyzer design. Descriptions of the individual circuits are found in the next section.

#### 4.1 Sounder Mode

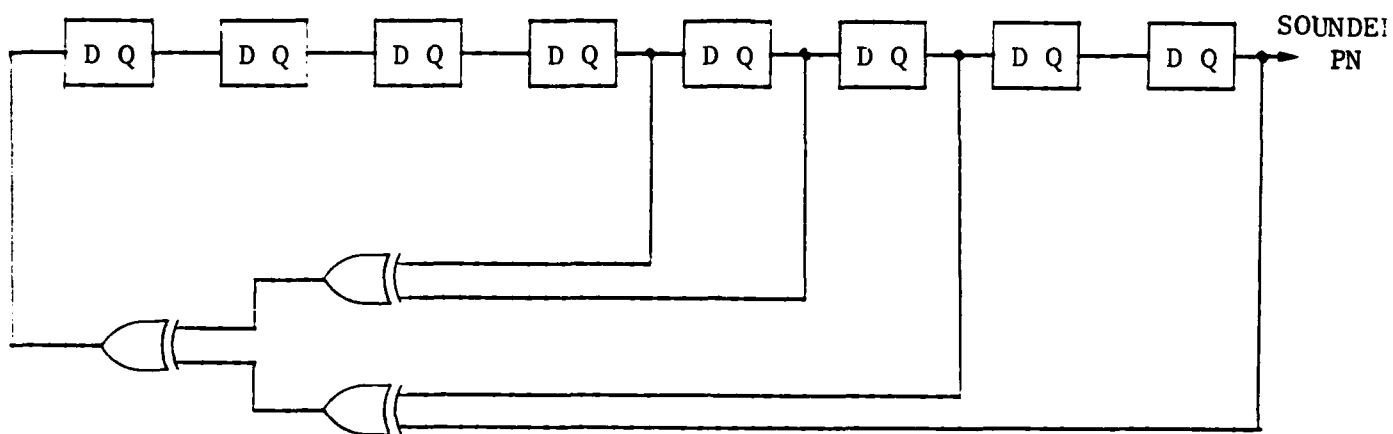
The Sounder Mode uses a 255 bit PN sequence as would be generated by the circuit shown in Figure 4.1. The transmitter pulse width is 8  $\mu$ s and the duty cycle is 25%. The analyzer samples the received waveform every 32  $\mu$ s. Each time a 255 bit sequence is received (or each N sequences if N sequences are integrated, N = 2, 4, 8), the sample clock is delayed by 4  $\mu$ s. The effective sampling rate is 250 kHz. The receiver is to have a 125 kHz filter in the Sounder Mode. 2040 tap gains are computed.

#### 4.2 Prober Mode

The Prober Mode uses a 2047 bit PN sequence as would be generated by the circuit shown in Figure 4.2. The transmitted pulse width is 1  $\mu$ s and the transmitter duty cycle is 25%. The analyzer samples every 4.0  $\mu$ s. The sampling clock is delayed by 0.5  $\mu$ s between each sequence or integration for an effective sampling rate of 2 MHz. The receiver has a 1 MHz filter. 16,376 tap gains are computed.

#### 4.3 Interfaces

Figure 4.3 shows the interfaces to the Wideband HF Channel Analyzer. The analyzer and the computer are linked by two



31.25 kHz CLOCK TO ALL FLIP-FLOPS

Figure 4.1 Sounder Mode PN Sequence Generator

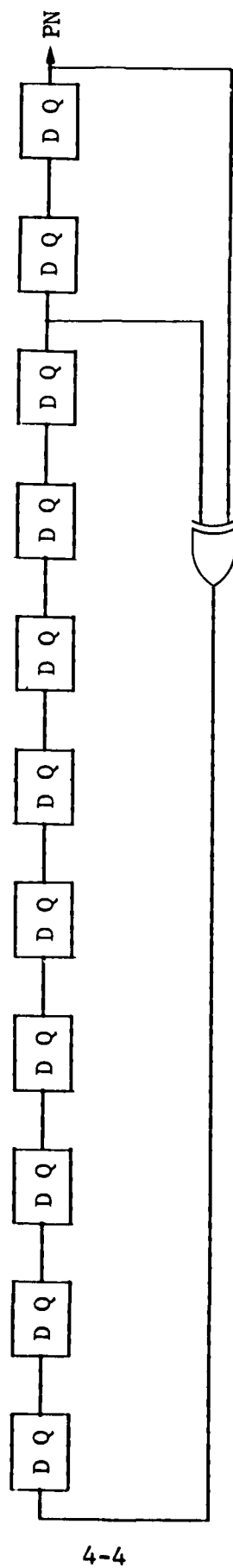


Figure 4.2 Prober Mode PN Sequence Generator

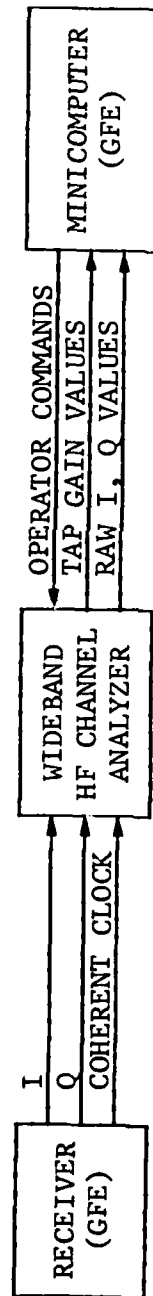


Figure 4.3 Wideband HF Channel Analyzer Interfaces

interfaces. One computer interface is bi-directional. This interface receives operator commands from the computer and transfers tap gain values to the computer. The other interface transmits raw I and Q samples to the computer for use in calculating an AGC level.

#### 4.4 Block Diagram

Figure 4.4 is the block diagram of the Wideband HF Channel Analyzer. The I and Q channels are identical and are controlled in parallel. Each channel consists of an analog-to-digital converter, integrating double buffer, and an array of digital correlators. The timing and control circuitry and the computer interface are shared by the I and Q channels.

The Timing and Control functions are performed by three circuit cards. Input Timing and Control, 58103, Correlator Control No. 1, 58106, and Correlator Control No. 2, 58107. Each Integrating Double Buffer is two 58102 Integrating Double Buffer Circuit Cards. There are eight 58101 Digital Correlator cards in the I channel and eight in the Q channel. Each Digital Correlator card has four correlator cells. What is shown as the computer interface in the block diagram includes the 58104 Computer Interface, 58108 FIFO Memory, and 58109 AGC Computer Interface. The A/D converters are on individual printed circuit cards.

#### 4.5 Operation

The analog input (I and Q) is sampled at a 250 kHz rate in the Prober Mode or a 31.25 kHz rate in the Sounder Mode. These samples are converted to two's complement digital values by the

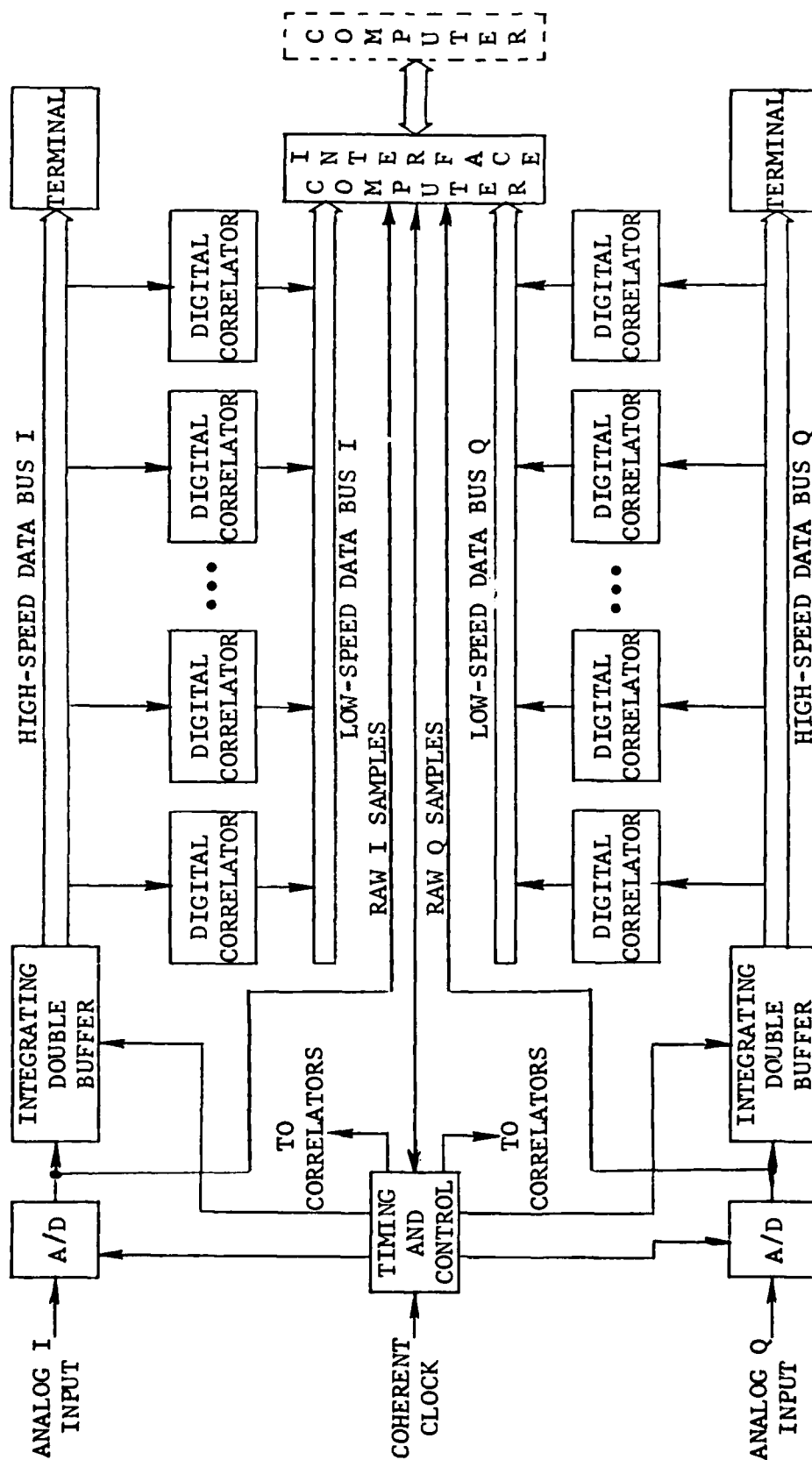


Figure 4.4 Block Diagram of Wideband HF Channel Analyzer

analog-to-digital converter and stored in the integrating double buffers.

Each integrating double buffer has two identical buffer memories. While one buffer is collecting input samples, the other buffer is being read into the correlators. When the desired input samples have been collected, the buffers exchange roles. The buffer taking input collects samples for the duration of one PN sequence. If several sequences are to be integrated, these samples are added to the next sequence received. Two, four, or eight sequences can be integrated for each mode. When the integration is complete (or if no integration was selected), the buffers exchange roles. The sampling clock is delayed by 0.5  $\mu$ s in the prober, or by 4  $\mu$ s in the sounder mode, before the first sample of the next sequence is taken.

The output of the integrating double buffers is fed to an array of high-speed digital correlator cells. There are 64 cells, 32 for I and 32 for Q. Each cell performs 64 correlations to correlate the input with all positions of the 2047-bit prober sequence.

In the Prober Mode, the basic PN sequence correlator performs the operation

$$\hat{g}_i = \sum_{k=0}^{2046} S_{k-i} r_k \quad (4.1)$$

where  $S_k$  are the PN sequence values, +1 or -1. In the sounder mode the operation is the same but the length is 255 ( $k = 0, 254$ ). To make the digital correlator hardware more efficient the terms of the sum are regrouped as

$$\hat{g}_i = c r_{2046} + \sum_{j=1}^{1023} a_j (r_{2j-1} + r_{2j-2}) + b_j (r_{2j-1} - r_{2j-2}) \quad (4.2)$$

where  $a_j$ ,  $b_j$  and  $c$  are obtained from  $S_{k-i}$  as follows:

$$c = S_{2046-i} \quad (4.3)$$

$$a_j = \frac{S_{2j-i-1} + S_{2j-i-2}}{2} \quad (4.4)$$

$$b_j = \frac{S_{2j-i-1} - S_{2j-i-2}}{2} \quad (4.5)$$

Either  $a_j$  or  $b_j$  is zero, and the nonzero coefficient  $a_j$  or  $b_j$  is +1 or -1. The coefficient  $c$  is +1 or -1.

The terms  $(r_{2j-1} + r_{2j-2})$  and  $(r_{2j-1} - r_{2j-2})$  are the sum and difference of two successive terms from the integrating double buffer. If the reference sequence,  $S_{k-i}$ , for these terms is (+1, +1) the sum is added into the correlation. If the reference is (-1, -1) the sum is subtracted. Similarly, for (+1, -1) the difference is added and for (-1, +1) the difference is subtracted.

Since  $(r_{2j-1} + r_{2j-2})$  and  $(r_{2j-1} - r_{2j-2})$  are input terms common to all the correlator cells in the I or Q array, the sum and difference are formed at the output of the integrating double buffer. Each correlator cell chooses one of the terms according to its reference sequence. The correlation summation requires 1023 time cycles for a 2047 bit sequence. The term  $c r_{2046}$  in (4.2) is forced into the correlator cell instead of an initial clear and, therefore, does not require an additional cycle.



The integrating double buffer performs a rate change. The input rate is 250 kHz in the prober mode and the output rate is 8 MHz. The output cycle is repeated 64 times for the 32 correlator cells in I and Q to perform the 2047 correlations. In the Sounder Mode the rates are 31.25 kHz and 1 MHz, respectively.

In the high data rate Prober Mode, 32 complex correlations are available every 128  $\mu$ s. The computer interface contains an output data preselector which compares the magnitudes of the I and Q voltage samples with a threshold and passes only those samples for which either or both magnitudes exceed the threshold.

Each eight cycles of 2047 correlations in the Prober Mode (65.5 ms) produce tap gain estimates for 16,376 taps spaced 0.5  $\mu$ s apart around an 8.188 ms delay ambiguity circle. The output data preselector deletes many samples for delay intervals which do not represent radio propagation paths and significantly decreases the computer memory and processing time requirements. The preselection threshold is selected by the computer to make the best possible use of the available computer processing capabilities.

Each transfer to the computer will be one or more blocks of three 16-bit words; a Tap Gain Index, an I voltage value, and a Q voltage value. Voltages will be 16-bit two's complement integers.

The identification of tap 0 by the hardware is not related to the radio propagation path, and computer software must scan all taps to determine the location of the earliest arriving signal. The preselection threshold logic will delete most tap gain samples and, typically, only a few hundred complex values will be transferred for each frame.

#### 4.6 System Arithmetic Scaling

The correlation computation requires a large number of arithmetic summations. If the samples are to be integrated before correlation, additional sums are required. System arithmetic scaling is controlled to prevent overflow in these operations. Scaling is done at the input of the Integrating Double Buffers according to the integration selected and at the input of the computer interface according to the mode of operation. Scaling at these points allows a fixed scaling on the high-speed data bus between the integrating double buffers and the correlator array.

The A/D converter is required to have 10 bits of precision. Integrating the A/D output for eight sequences requires an additional 3 bits. The correlator cells require 24-bit arithmetic units because the growth for the sum of 2047 samples is 11 bits. Since one sum is done in the integrating double buffer, the input to the correlator cells is 14 bits precision with 10 bits of sign extension. This scaling is fixed and the input to the integrating double buffer is shifted to maintain this scaling. The A/D converters are 12-bit units. This additional precision is carried through the integrating double buffers and, for an integration less than eight sequences, into the correlators.

The I and Q data sent to the computer is 16 bits precision. There is a difference of 3 bits in the scaling between the Sounder and Prober Modes due to the smaller growth factor in the Sounder Mode. The 16 bits to be sent to the computer are selected at the computer interface.

Figure 4.5 shows the arithmetic scaling for the Wideband HF Channel Analyzer.

A/D CONVERTER OUTPUT		$\begin{matrix} 11 \\ 10 \end{matrix} 9876543210$
INPUT TO INTEGRATING DOUBLE BUFFER	$\int = 1$	$E \begin{matrix} 11 \\ 10 \end{matrix} 9876543210 FFF$
	$\int = 2$	$EE \begin{matrix} 11 \\ 10 \end{matrix} 9876543210 FF$
	$\int = 4$	$EEE \begin{matrix} 11 \\ 10 \end{matrix} 9876543210 F$
	$\int = 8$	$EEEE \begin{matrix} 11 \\ 10 \end{matrix} 9876543210$
INPUTS TO CORRELATOR		
	UPS	$\begin{matrix} 111 \\ 210 \end{matrix} 9876543210$
	SUM,DIF	$\begin{matrix} 1111 \\ 3210 \end{matrix} 9876543210$
CORRELATOR OUTPUTS		
		$\begin{matrix} 22221111111111 \\ 32109876543210 \end{matrix} 9876543210$
INPUT TO COMPUTER INTERFACE		
SOUNDER		$\begin{matrix} 111111 \\ 543210 \end{matrix} 9876543210$
THRESHOLD		$\begin{matrix} 11 \\ 10 \end{matrix} 9876543210$
PROBER		$\begin{matrix} 111111 \\ 543210 \end{matrix} 9876543210$
THRESHOLD		$\begin{matrix} 11 \\ 10 \end{matrix} 9876543210$
E = SIGN EXTENSION		
F = ZERO FILL		

Figure 4.5 Wideband HF Channel Analyzer System Scaling

## SECTION 5

### CIRCUIT DESCRIPTIONS

This section describes each circuit in the Wideband HF Channel Analyzer. References are made to the schematic diagrams which accompany this report.

#### 5.1 Digital Correlator, 58101

The Digital Correlator circuit has four correlator cells with shared data buses at the input and output. Each cell is a 24-bit arithmetic unit with multiplexing registers at both inputs. Cells are controlled individually from Correlator Control No. 1, 58106, and Correlator Control No. 2, 58107. Eight digital correlator cards are used for the I channel and eight for the Q channel.

The Digital Correlator circuit is shown on SD58101. The control signals for the correlator cells are received and buffered on SD58101, p. 3. IM - DM are multiplexer control signals. These control lines are terminated for increased noise immunity. The signals CAS0 - CDS1 are arithmetic control lines and are reclocked.

The input data bus receivers are shown on SD58101, p. 4. Input data is from the Integrating Double Buffers. The SUM and DIF buses are from the arithmetic section at the output of the Integrating Double Buffer memory. The UPS (unpaired sample) bus is from the integrator trap register.

Correlator cell A is shown on SD58101, p. 5. The correlation is computed by adding or subtracting the sum or difference of a pair of samples from the previous sum. The unpaired

sample is forced into the accumulator at the start of the correlation instead of an initial clear.

The arithmetic unit uses 74S381 high-speed arithmetic logic units (ALU's) and 74S182 carry look-aheads. The arithmetic unit performs the functions  $A+B$ ,  $A-B$ , and  $B-A$  under control of AS0 and AS1. The A input to the ALU is the accumulated value or, initially, the unpaired sample (UPS) from the multiplexing register controlled by SELUPS. The B input to the ALU is from the multiplexing register controlled by ASEL and is either the SUM or DIF from the Integrating Double Buffer.

Correlator cells B, C, and D are shown on SD58101, pp. 6, 7, and 8. The output registers for all four cells are shown on SD58101, p. 10. The cell outputs are first multiplexed onto a local bus, COR23 - COR0, and then onto the TG bus using drivers shown on SD58101, p. 11.

A cell's output is enabled onto the TG bus by an address from the Computer Interface, 58104. The five-bit address, BAD4 - BAD0, is decoded by the circuit shown on SD58101, p. 9. The three MSB's of the address are decoded to  $\overline{BD0}$  -  $\overline{BD7}$ . One of these signals is tied to  $\overline{BDEC}$  on SD58101, p. 10, by a backplane jumper. Thus, the address of the board is determined by its location. The two LSB's of the address select one of the four cells.

## 5.2 Integrating Double Buffer, 58102

The Integrating Double Buffer is a double buffer memory with processing at the input and output. One buffer operates in the data collection mode while the other operates in the data output mode. When the data collection operation is complete the buffers exchange roles. Each Integrating Double Buffer card can process up to eight bits of data. In the Wideband HF Channel Analyzer, two cards are used for the I channel and two for the Q channel.

The Integrating Double Buffer circuit is shown on SD58102. Four gated clocks are shown on SD58102, p. 2. Input processing is done at the A/D converter rate. INCLK is the system clock gated at the A/D rate. Output processing is done at the correlator rate. OUTCLK is the system clock gated at the correlator rate. The memories must operate at one rate during their input cycle and the other during their output cycle. MEMCKA and MEMCKB are alternately switched between INCKGT and OTCKGT by the buffer toggle, BUFSEL.

The data from the A/D is scaled by the shifting circuit shown on SD58102, p. 2. The shift code, SC1 SC0, is set by the Input Timing and Control Board according to the number of sequences to be integrated. The scaling at the output of the Integrating Double Buffer is fixed.

The scaled data is clocked into the integrator shown on SD58102, p. 4. The integrator is an eight bit adder with registers at the input and output. The carry in and carry out of the adder are brought to the card edge connector so that

two Integrating Double Buffer cards can be tied together for sixteen bit precision. The second input to the adder comes from memory. This input can be forced to zero with the STROBE signal. A second feedback path controlled by BITINT is not used. The output of the integrator goes to the memory. A second output register controlled by TRAPEN traps the last sample integrated. This sample is sent directly to the correlators. The even number of samples remaining in memory will be processed in pairs.

Page 5 of SD58102 shows the addressing and write strobe generation for the memories on pages 6, 7, 8, and 9. Two memories, identified by the prefixes A and B on signal names, form the double buffer. Each of these memories is further divided into an upper and lower part, AU, AL, BU, and BL. The four memories are operated as RAM shift registers of length 127 in the sounder mode or length 1023 in the prober mode. The length of the memory is determined by N9 - N0. Operation of the memories is controlled by the Input Timing and Control Board, 58103, through the enables AUEN - BLEN and the write enables, AUWRT - BLWRT.

During an input cycle, data is alternately written into upper and lower memory and read from lower and upper at the input rate. This forms a shift register of length 254 in the sounder mode or length 2046 in the prober mode. The remaining sample is held in the integrator. The AND gates shown on SD58102, p. 10 pick the bit from the memory being read (upper or lower) because the memory output is high during a write cycle. The multiplexer on the same page chooses the

A or B memory output to be fed back to the integrator. If STROBE is high, the feedback is forced to 0.

For an output cycle, the enables for the upper and lower parts of the A or B memory are held high and the write enables are held low. The integrated samples are read in pairs at the output rate. The contents of the memory are read once for each pass of the correlator array, 8 times in the sounder mode, 64 times in the prober mode.

The arithmetic units shown on SD58102, p. 11, form the sum and difference of each sample pair as it is read from memory during an output cycle. Again, the carry in and carry out of each adder is brought to the card edge for expansion. The sums and differences are reclocked and buffered for transmission to the correlators.

### 5.3 Input Timing and Control Board, 58103

The Input Timing and Control Board generates the timing and control signals required by the A/D converters and the Integrating Double Buffers. The external 8 MHz coherent clock is buffered on the Input Timing and Control Board and distributed to the other circuits in the Wideband HF Channel Analyzer.

Although all processing in the Wideband HF Channel Analyzer is synchronous with the 8 MHz clock, the various processing steps occur at different rates. Each step of the processing is input driven; that is, when one step is complete, the next step is commanded to start. The design is such that each step will be ready to process data when the input data for that step is ready.



The first step of processing channel data is an analog-to-digital conversion. The A/D converters are controlled by the pulse signal  $\overline{\text{CONV}}$ .  $\overline{\text{CONV}}$  is generated by the circuitry shown on SD58103, pp. 3 and 4. Several other control signals and reference markers are generated relative to  $\overline{\text{CONV}}$ . These signals will be referred to as sample-time signals since they are referenced to the sampling of the analog input to the analyzer.

The counter chain shown on SD58103, p. 3, produces three sample-time signals, SAMPLE, SLAST, and ILAST. SAMPLE is a pulse signal generated by dividing the 8 MHz clock to the bit rate of the PN sequence (31.25 kHz in the sounder mode or 250 kHz in the prober mode).  $\overline{\text{CONV}}$  is generated from SAMPLE using a pulse stretching circuit to meet the requirements of the A/D converters.

The sample counter counts SAMPLE pulses and produces a pulse signal, SLAST, coincident with SAMPLE for the last sample of the input sequence (255 samples in the sounder mode, 2047 samples in the prober mode). The sequence counter counts the sequences to be integrated (1, 2, 4 or 8) and produces a pulse signal ILAST coincident with SAMPLE and SLAST. ILAST marks the last sample of the last sequence to be integrated.

ILAST is fed back through a delay equal to  $1/8$  chip. The output of the delay is used to reset the clock to sample rate divider which delays sampling the next input sequence by  $1/8$  chip. The feedback delay is called a time multiplexer delay because the effect is the same as switching the sample clock between sources of different phases. The output of the time multiplexer delay is also used to increment a three-bit counter. These three bits are the frame index of the input data.

The other reference marker generated in sample-time is the correlator reference address, RA10 - RA0. The reference address is used as a starting point for the correlator array. The reference address is generated by sampling a coherent counter when the first sample of an input sequence is taken. The reference address circuitry is shown on SD58103, pp. 6 and 7. There are two coherent counters. The prober mode counter counts 0 to 2046 at a 250 kHz rate and the sounder mode counter counts 0 to 254 at a 31.25 kHz rate.

Two flip-flops on SD58103, p. 3, generate ENSMP from the terminal count of the coherent reference counter for the mode selected. ENSMP enables the clock to sample rate divider in synchronism with the reference counter. ENSMP and RA10 - RA0 assure consistent indexing of the tap gain values.

The PN sequence PROM's shown on SD58103, p. 8, were used for testing. Similarly, the coherent counters terminal count pulses,  $\overline{\text{PRSYNC}}$  and  $\overline{\text{SDSYNC}}$ , are buffered and made available as  $\overline{\text{PRSNC}}$  and  $\overline{\text{SDSNC}}$  for testing.

The preceeding signals are generated in sample-time; that is, relative to the input to the A/D converter. The A/D converter requires slightly more than 2  $\mu\text{sec}$  to perform the conversion. The sample-time signals required to control input processing are delayed by the shift registers shown on SD58103, p. 4. This is a fixed 3  $\mu\text{sec}$  delay.

The control signals for the Integrating Double Buffers are generated by the circuits shown on SD58103, p. 5. SMPLD is SAMPLE delayed by 3  $\mu\text{sec}$ . SMPLD is buffered and used as the

input clock gate, INCKGT. The clear line to the clock to sample rate divider, ICL, delayed is ICLD. ICLD is used to generate the buffer toggle, BUFSEL, and the start correlation command, STCOR.

The integration code ICOD2 - ICOD0 is converted to a shift code S1, S0 for scaling the data at the input to the Integrating Double Buffers. The remainder of the signals shown on SD5103, p. 5, are enables described in Section 5.2, Integrating Double Buffer, 58102.

System clock distribution is shown on SD58103, p. 9. The 8 MHz external clock is buffered and distributed as  $\overline{\text{CLK1}}$  -  $\overline{\text{CLK23}}$ . An individual terminated twisted pair is run to each board receiving system clock. The bar designation is a notational convenience used because the clock receivers are inverting. All registers are clocked on the rising edge of the local clock which is the falling edge of the distributed  $\overline{\text{CLK}}$ .  $\overline{\text{CLK}}$  may be gated at the receiver. There is always one gate delay between the  $\overline{\text{CLK}}$  and the local clock. CLOCKS, CLOCKS, CLOCKS, and CLOCKS are the local clocks on 58103.

#### 5.4 Computer Interface, 58104

The 58104 Computer Interface is the primary interface between the Wideband HF Channel Analyzer and the system computer. The 58104 Computer Interface receives mode, integration, and threshold data from the computer. The CSR1 bit received by this interface sets the analyzer to the active state. When active, the computer interface reads data from the correlator array, tags the data with a tap gain index, compares the data with a threshold, and, if the data exceeds

the threshold, writes the data into the 58108 FIFO memory. When data is available at the output of the FIFO, the Computer Interface generates REQA to the system computer. The 58104 Computer Interface is designed to work with a DEC DR11-C interface in the system computer.

Data from the system computer, OUT00 - OUT15, New Data Ready, and CSR1, are shown on SD58104, p. 3. CSR1 high puts the analyzer into the active state and CSR1 low puts the analyzer into the idle state. CSR1 is reclocked at the interface for synchronous operation. New Data Ready is a pulse signal from the DR11-C which indicates that OUT00 - OUT15 have changed. New Data Ready is used to strobe the data through a set of double latches which prevents transient data from entering the analyzer. The latches containing mode and integration data are disabled when the analyzer is in the active state. Threshold data can be changed in either the active or idle state.

At the end of a correlation pass, the data from the 32 I and 32 Q correlator cells is read by addressing the cells as shown on SD58104, p. 4. When data has been transferred to the correlator output registers as indicated by CRCKGT and OUTGT, the address counter is cleared and enabled. The address counter counts 0 to 31 to read all the cells and stops. If it is the last pass, an end of frame,  $\overline{\text{EOF}}$ , is generated when the last cell is read. The address counter output is inverted at the computer interface and then on the correlator cards with Schmidt trigger gates for noise immunity. The inverted address is used as part of the tap gain index because the tap with the greatest delay is computed by cell 0.

Addressing a correlator cell enables the tap gain data from that cell onto the I or Q data bus. The corresponding I and Q cells are read in parallel. Bus receivers for the I and Q buses are shown on SD58104, p. 5. The bus terminating resistors are shown on SD58104, p. 6. Each correlator has 24 bits precision. Only the 16 most significant bits are sent to the computer. In the sounder mode, the three MSB's from the correlator are sign extension due to the shorter sounder mode sequence. The 16 most significant bits for either mode are selected by using the tri-state outputs of the bus receivers as a multiplexer. The selected bits are reclocked for possible transfer to the FIFO memory.

The I and Q values from the correlator array are compared to the threshold value from the computer as shown on SD58104, p. 6. The threshold, a 12-bit unsigned positive integer, is applied to the A input of an ALU. ALU operation is controlled by the sign bit of the correlator output. If the correlator output is negative, the operation  $A + B$  is performed. If the correlator output is positive  $A - B$  is used. In either case, if the result is negative, as indicated by a 0 carry into what would be the sign bit, the correlator output exceeds the threshold. Note that this is a "strictly greater than" comparison.

If either the I or Q value exceeds threshold or if an end of frame marker was generated the I value, Q value and tap gain index are strobed into the FIFO memory. The Tap

Gain Index is a concatenation of the frame index, the cell address (inverted), and the correlator pass count (inverted). Bit 15 of the Tap Gain Index is set to indicate valid data and bit 14 is the end of frame marker. The Tap Gain Index, TGI15 - TGI0, I value, IO15 - IO0, and Q value, QO15 - QO0 are held in registers connected to the FIFO input. If the conditions for transfer are met, the Computer Interface generates a parallel load command,  $\overline{PL}$ , to strobe the data into the FIFO (SD58104, p. 7).

The FIFO memory, 58108, is actually three memories which are loaded in parallel and read sequentially under control of the Computer Interface. When data is present at the output of all three memories (AORE, BORE, CORE all low), the Computer Interface generates REQA and enables the Tap Gain Index onto the input lines to the system computer. When the computer has taken the data as indicated by a DATA TRANS pulse, the interface enables the I tap gain value. The next DATA TRANS pulse enables the Q tap gain value. After the Q value has been transferred, the interface checks the FIFO output. If there is additional data present at the FIFO output, the transfer is continued; otherwise, REQA is dropped.

#### 5.5 A/D Converter, 58105

The analog-to-digital converter circuit uses the Datel SHM-5 sample-hold and the Datel ADC-EH12B3 analog-to-digital converter. The circuit, shown on SD58105, is from the Datel application notes with additional buffering for device protection and additional noise immunity. Adjustment of the A/D converter is described in Appendix A. The A/D converter circuit is fabricated on a printed circuit card. The A/D converter card must not be removed from the card cage with power applied.

The analog input is brought onto the card through an SMA connector, J3. Space is provided on the printed circuit card for an optional terminating resistor. The SHM-5 sample-hold is inverting so a negative input voltage produces a positive binary value from the A/D. The sample control of the SHM-5 is set by the status (EOC) output of the A/D converter through an inverter. The sample-hold is in the track mode except when a conversion is in process.

A conversion is initiated by an active low pulse on either  $\overline{\text{CONV1}}$  or  $\overline{\text{CONV2}}$ . In the Wideband HF Channel Analyzer,  $\overline{\text{CONV1}}$  is generated by the Input Timing and Control Board.  $\overline{\text{CONV2}}$  is from the AGC computer interface.  $\overline{\text{CONV1}}$  is generated when the analyzer is in the active state.  $\overline{\text{CONV2}}$  can be generated only when the analyzer is in the idle state.

The ADC-EH12B3 is biased to produce a bipolar output. The  $\overline{\text{MSB}}$  output is used to obtain a two's complement code. All outputs of the A/D are buffered and brought out to the card edge connector. This buffering provides additional drive capability and also protects the ADC-EH12B3 from accidental short circuits on the backplane.

#### 5.6 Correlator Control No. 1, 58106

Correlator Control No. 1 has the reference PN sequence ROMs for the sounder and prober modes and also generates the non-arithmetic control signals required by the correlators. The arithmetic control signals are generated from the reference PN sequences by Correlator Control No. 2, 58107.

Correlator Control No. 1 is shown on SD58106. Control signals are generated by the circuits on SD58106, p. 3.

The correlation process is started by the pulse signal STCOR from the Input Timing and Control Board, 58103. STCOR starts the sequential initialization and enabling of several counters. This sequencing allows the current correlation to complete while the next correlation is starting in a fully pipelined process.

The sample pair counter determines when a correlation pass is complete and causes the result to be transferred to the correlator output registers by generating OUTGT. In the sounder mode, 127 pairs are processed. The prober mode requires 1023 sample pairs per pass. There are 32 correlator cells on eight boards computing correlations in parallel in both the I and Q channels. Eight passes are required to compute all correlations in the sounder mode and sixty-four in the prober mode.

The correlator pass counter is incremented each time the sample pair counter determines that a pass is complete. The pass count becomes part of the tap gain index. When the last pass is complete, OUTGT is inhibited and LSTPAS goes high. LSTPAS is used by the Computer Interface, 58104, to generate the end of frame marker.

The correlator clock divider shown on SD58106, p. 3, generates the correlator clock gate, CRCKG. In the prober mode, the correlators are run at the 8 MHz system clock rate and CRCKGT is high. In the sounder mode, the correlators are run at a 1 MHz rate.

Prober mode ROM addressing is shown on SD58106, p. 4. The prober mode ROMs are shown on SD58106, p. 6. Sounder



mode ROM addressing is shown on SD58106, p. 5, and the ROMs on page 7. The reference PN sequences are buffered on SD58106, p. 8.

Three phases of the PN sequence are used to generate the arithmetic control for each cell. The control of correlator cell 0 is generated from PN0, PN1, and PN2 which can be written as  $PN(t+0)$ ,  $PN(t+1)$ , and  $PN(t+2)$ . PN0 is used to correlate the unpaired sample which is the last sample received. PN1 and PN2 are used to correlate the sums and differences of sample pairs  $(x_1 \pm x_0)$ ,  $(x_3 \pm x_2)$ , etc. The reference sequences for correlator cell 1 are PN1, PN2 and PN3. Thirty-four phases of the PN sequence, PN0 - PN33, are required for the thirty-two correlator cells.

Note that PN0 represents the sequence with the most delay. Adding a positive offset to the ROM address (mod 255 or mod 2047) generates reference sequences with less delay,  $PN(0+t+OFFSET)$ . The thirty-two correlations representing the greatest delay are computed first then an offset of 32 is added to the ROM base address and the next thirty-two correlations are computed. The process is repeated until all delays have been computed.

The ROM address generator for the prober mode is shown on SD58106, p. 4. At the start of a correlation, the reference address, RA0 - RA10, from the coherent counter on 58103 is loaded into the first counter by  $\overline{LOAD1}$ .  $\overline{LOAD2}$  transfers this starting address into the second counter which addresses the ROMs.  $\overline{LOAD2}$  also causes the first counter to increment by 32 in preparation for the next pass. The second counter counts mod 2047 by 2's. Since two reference sequences are used to

correlate pairs of samples, only alternate bits of each reference are required. At the end of the first pass, the new starting address is loaded into the second counter and the first counter is incremented by 32 mod 2047. This process is repeated for the sixty-four passes in the prober mode.

Sounder mode PN ROM addressing is shown on SD58106, p. 5. These counters operate the same as the prober mode counters but count mod 255.

#### 5.7 Correlator Control No. 2, 58107

Correlator Control No. 2 converts the reference PN sequences from Correlator Control No. 1 into control signals for the correlator cells. The Correlator Control No. 2 circuit is shown on SD58107.

Each correlator cell requires two arithmetic control signals and two multiplexer control signals. One multiplexer control signal initializes the accumulator registers to the unpaired sample value and is common to all cells. This multiplexer control signal is generated on Correlator Control No. 1. The other multiplexer control signal switches the B input of the correlator ALU between the SUM and DIF outputs of the Integrating Double Buffer and is unique for each cell. The circuits which generate these control signals are shown on SD58107, p. 3.

If the reference bits for a pair of samples are (1,1) or (0,0), the sum of the samples is added or subtracted from the accumulator. If the reference bits are (1,0) or (0,1), the difference is added or subtracted. Thus, the control signal required to select between the SUM and DIF data buses is the exclusive OR of the reference bits.

The arithmetic unit in a correlator cell can perform the operations  $A + B$ ,  $A - B$ , and  $B - A$ . The A input is initially the unpaired sample. After initialization, the A input register becomes an accumulator. The B input is from either the SUM or DIF buses as described above. Except for one special case described below, only the operations  $A + B$  and  $A - B$  are used. For these operations, the S1 control line is high and the S0 control line is high for  $A + B$  and low for  $A - B$ . Except for the special case, S0 is controlled directly by a PN sequence.

The special case arises when the accumulator register is initialized to the unpaired sample. For some sequences, the desired operation is  $-A - B$ . Since this operation is not available,  $A + B$  is used and a flip-flop is set to indicate that the accumulator has the wrong sign. The correlation proceeds with the operation  $A + B$  substituted for  $A - B$ . When the operation  $A + B$  is encountered, the operation  $-A + B$  is substituted to correct the sign of the accumulator. The correlation then proceeds normally using only the operations  $A + B$  and  $A - B$ .

The circuits used to generate the arithmetic controls for the correlator array are shown on SD58107, pp. 4 - 11. The controls for the four cells on one Digital Correlator card are shown on each page.

## 5.8 FIFO Memory, 58108

The First-In First-Out Memory, or FIFO, is a buffer between the Wideband HF Channel Analyzer and the system computer. Data is written into the memory in a high-speed burst mode by the analyzer and read at a slower rate by the computer.

The circuit diagram for the FIFO Memory is shown on SD58108. The circuit is actually three identical, independent FIFO memories built on one circuit card. The three memories are used for the Tap Gain Index, I tap gain, and Q tap gain outputs of the analyzer. The memories are loaded in parallel and read sequentially. The design is such that the total amount of FIFO memory can be expanded by adding an additional 58108 card.

The circuit design is based on the Fairchild 9423 integrated circuit which is a 64 x 4 bit FIFO memory. The interconnection is a vertical and horizontal expansion to make a 256 x 16 FIFO. The 9423 has an input register, a fall-through stack and an output register. Data is loaded into the input register by PL and transferred to the stack by  $\overline{TTS}$ . Once in the stack, the data occupies the lowest available position. Data at the lowest position in the stack is transferred to the output register by TOP. When a datum is removed from the stack by a TOP, any data still in the stack moves down by one position.

The interconnection shown makes all transfers automatic except for the PL at the input of the FIFO and the TOP at the output. The initial PL and final TOP are generated by the Computer Interface, 58104. The ORE (output register empty) signal is used by the Computer Interface to detect when there is data present to transfer to the computer. The tri-state buffers at the output of each FIFO are used to multiplex the Tap Gain Index, I tap gain, and Q tap gain onto the computer input bus.

The FIFO will overflow if the computer does not read out the data at the same average rate as the analyzer writes into

the FIFO. A threshold comparison is used to control the amount of data generated by the analyzer. The FIFO overflows at the input. Only the new data is lost. Data previously in the FIFO stack remains valid. The one data word in the FIFO input register may be partially overwritten and is, therefore, unreliable. The master reset,  $\overline{MR}$ , is used to clear the FIFO of any random data when the analyzer is in the idle state.

#### 5.9 AGC Computer Interface, 58109

The AGC Computer Interface is a simple interface circuit which allows the system computer to sample the analog I and Q inputs to the Wideband HF Channel Analyzer. The AGC Computer Interface is designed to work with a DEC DR11-C interface in the system computer.

The AGC Computer Interface is shown on SD58109. The analyzer must be in the idle state for the interface to respond to the DR11-C. The interface is operated from the computer by reading the input register of the DR11-C. Reading the input register generates the pulse signal DATA TRANS. The data from the first read should be ignored. The register is read to generate DATA TRANS.

DATA TRANS triggers a one-shot which generates a convert command,  $\overline{CONV}$ , to the I and Q channel A/D converters. When the A/D conversions are complete, REQA is asserted. The A/D converter outputs are now present at the DR11-C input register. Eight bits of I data and eight bits of Q data are packed into the 16-bit word IN15 - IN0. Q7 - Q0 are in IN15 - IN08 and J7 - J0 in IN07 - IN00. Reading the DR11-C input register generates another DATA TRANS pulse and initiates a new conversion. Conversions can be performed at the maximum data rate of the DR11-C.

## APPENDIX A

### ADJUSTMENT OF A/D CONVERTER

The following describes the procedure for adjusting the gain and offset of the 58105 analog-to-digital converter. This procedure requires the following test equipment:

- (1) A stable, adjustable voltage source with  $\pm 5$  vdc range. A stable power supply and a multi-turn potentiometer are recommended.
- (2) A digital voltmeter with five decimal digits precision (capable of measuring 5 vdc to 0.1 mv).
- (3) A dual-trace laboratory oscilloscope.
- (4) An SMA-type shorting cap.
- (5) A cable with an SMA-type connector to connect the adjustable voltage source to the A/D converter.

In addition, the system computer will be used to strobe the A/D converters through the AGC Computer Interface. A small program should be written to set the analyzer to the IDLE state and to repeatedly strobe the A/D by reading its output through the AGC Computer Interface.

The component side of the 58105 A/D converter is shown in Figure 1.

#### Adjustment Procedure

##### I. Setup

- (1) With the power turned off, disconnect the input coaxial cable to the A/D converter to be adjusted

and put the converter on an extender board.

\* \* \* \* \*

\* Caution: The 58105 A/D converter must not be \*

\* removed or inserted when power is on or damage \*

\* to the unit may occur. \*

\* \* \* \* \*

- (2) Run the test program on the system computer.

## II. Sample-Hold Offset Adjustment

- (1) Place shorting cap on J3.
- (2) Connect digital voltmeter to SHM-5 pin 16 and ground (both sides of the printed circuit board are ground plane).
- (3) Adjust R2 for 0 volts offset.

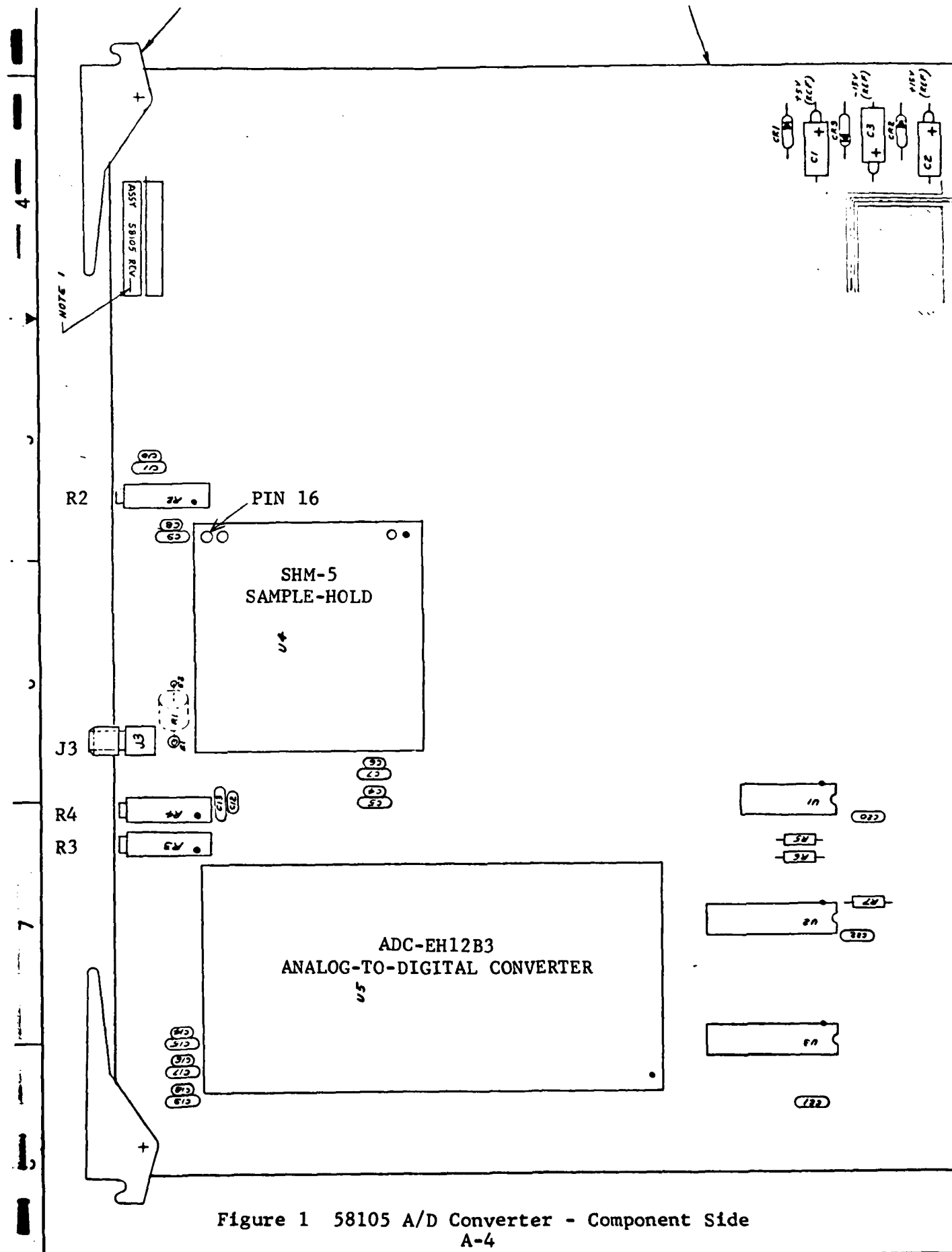
## III. A/D Offset Adjustment

- (1) Connect the trigger input of the oscilloscope to P2 C33, EOC. Set the oscilloscope to trigger on the rising edge of EOC.
- (2) Connect Channel 1 of the oscilloscope to P2 C32, SDCK.
- (3) Connect Channel 2 of the oscilloscope to P2 C30, SDATA.
- (4) Apply +4.9988 vdc to J3.
- (5) Adjust R4 to obtain the waveform shown in Figure 2A.

IV. A/D Gain Adjustment

- (1) Oscilloscope is connected as in Part III.
- (2) Apply -4.9963 vdc to J3.
- (3) Adjust R3 to obtain the waveform shown in Figure 2B.





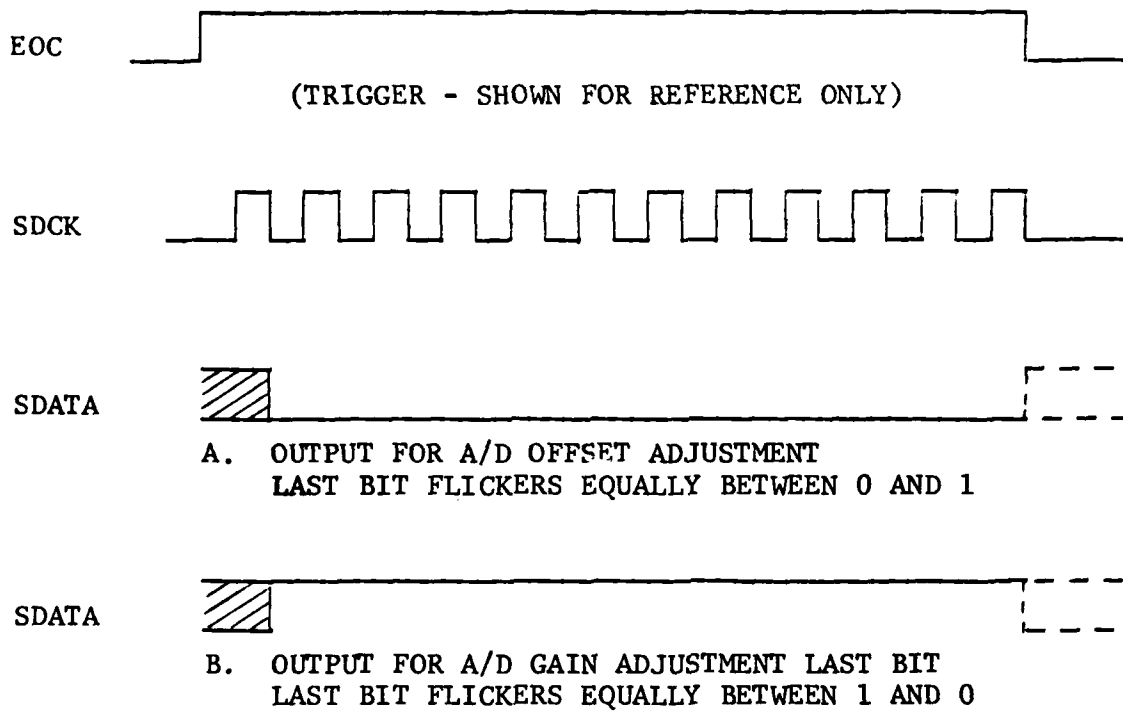


Figure 2 A/D Output Waveforms

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